REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application and indicating the claims 8, 19, and 30 are allowable.

I. Disposition of Claims

Claims 1-33 are currently pending in the present application. By way of this reply, claims 1, 12, and 23 have been amended.

II. Claim Amendments

Claims 1, 12, and 23 have been amended to clarify that the operation of the phase locked loop is simulated prior to fabrication of the phase locked loop. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in paragraph [0030] of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1-7, 9-18, 20-29, and 31-33 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by Jenkins et al. ("Measuring Jitter and Phase Error in Microprocessor Phase-Locked Loops," Keith A. Jenkins and James P. Eckhardt, IEEE Design and Test of Computers, April – June 2000, pages 86-93). For the reasons set forth below, this rejection is respectively traversed.

The present invention is directed to a technique for estimating/determining jitter of a phase locked loop based on a simulation of the phase locked loop. *See* Specification,

paragraph [0025]. With reference to the exemplary flow process shown in Figure 5a of the present application, a technique in accordance with the present invention involves (i) obtaining a representative power supply waveform having noise **172**, (ii) digitizing the representative power supply waveform having noise **174**, and (iii) simulating operation of a phase locked loop using the digitized representative power supply waveform having noise as a power supply input to the phase locked loop **176** (*see also* Specification, paragraph [0028]).

The simulation of the operation of the phase locked loop occurs prior to actual fabrication of the phase locked loop. *See, e.g.*, Specification [0030] (referring to an "intended" location of a PLL). In such a manner, a designer is able to observe the effects of a power supply on a designed phase locked loop before actual fabrication of the phase locked loop on an integrated circuit. Otherwise, if a fabricated phase locked loop is found to be adversely affected by the power supply components of the integrated circuit on which the phase locked loop is fabricated, valuable space and resources are wasted.

Accordingly, amended independent claims 1, 12, and 23 of the present application have been amended to clarify that the simulation of the phase locked loop occurs prior to actual fabrication of the phase locked loop. Applicant notes that these amendments are clarifying in nature in that references to "simulation" prior to the amendments were intended to define simulation in the ordinary sense of the term as it used in integrated circuit design, i.e., as occurring prior to fabrication. Thus, no further search is believed to be required.

Jenkins, in contrast to the present invention, fails to at least disclose the limitations discussed above. In Jenkins, the phase locked loop is fabricated prior to the

purported "simulation." *See* Jenkins, page 89, column 1, lines 8 – 14 ("We use a combination of noise generation circuits *fabricated* along with the PLL . . .") (emphasis added); *see also* Jenkins, Figure 6 (caption reading "[t]he noise generator is integrated into the PLL macro, *on the wafer*) (emphasis added). Thus, in Jenkins, if the power supply components of the system are found to adversely affect the purported phase locked loop to the point of malfunction or poor performance, expensive re-design and re-fabrication of the phase locked loop are required.

As indicated throughout the present application, an important aspect of the claimed invention is to capture a power supply waveform from a physical system and apply that waveform, in digitized form, to a simulated phase locked loop so that the operation of the phase locked loop may be determined, possibly under various operating conditions, *prior to actual fabrication* of the phase locked loop. *See* Specification, paragraph [0030]. Instead, in Jenkins, as discussed above, the purported phase locked loop is fabricated prior to the purported simulation of the phase locked loop. Thus, Jenkins fails to disclose simulating operation of the phase locked loop prior to fabrication of the phase locked loop as required by amended independent claims 1, 12, and 23 of the present application.

In view of the above, Jenkins fails to show or suggest the present invention as recited in amended independent claims 1, 12, and 23 of the present application. Thus, amended independent claims 1, 12, and 23 are patentable over Jenkins. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

The above amendments and remarks are believed to require no further prior art search. Also, Applicant believes that this reply is responsive to all outstanding issues and places the referenced application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Because the amendments and remarks simplify the issues for allowance or appeal, and do not constitute new matter, entry and consideration thereof is respectfully requested.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.170001;P7188).

Respectfully submitted,

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